Patent Claims

1. A memory arrangement having rewritable memory cells (MC) which are arranged at crossovers between word lines (WL) and bit lines (BL), in which arrangement the memory cells (MC) are configured in such a manner that the information stored in the memory cells (MC) is essentially read out in a nondestructive manner,
wherein
the memory arrangement has a flag cell (MMC) either for each word line (WL) or for each bit line (BL), said flag cell being able to store an item of information that indicates whether at least one of the memory cells (MC) either along the respective word line (WL) or along the respective bit line (BL) has been subjected to a reading operation since a basic state occurred.

2. The memory arrangement as claimed in claim 1,
wherein
the flag cells (MMC) are of the same memory cell type as the memory cells (MC).

3. The memory arrangement as claimed in claim 1 or 2,
wherein
the flag cells (MMC) are of a memory cell type in which the stored information can be read out in a nondestructive manner.

4. The memory arrangement as claimed in one of the preceding claims,
wherein
the flag cells (MMC) are of the nonvolatile type.

5. The memory arrangement as claimed in one of the preceding claims,
wherein

the memory arrangement is an individual memory chip (MEM).

6. The memory arrangement as claimed in one of the preceding claims,
wherein
the memory arrangement is a plurality of memory chips (MEM) which are assigned to one another.

7. The memory arrangement as claimed in one of the preceding claims,
wherein
the memory arrangement has a refresh device (Refr) for carrying out a refresh operation.

8. A method for operating a memory arrangement having rewritable memory cells (MC) which are arranged at crossovers between word lines (WL) and bit lines (BL), in which arrangement the memory cells (MC) are configured in such a manner that the information stored in the memory cells (MC) is essentially read out in a nondestructive manner,
wherein
those memory cells (MC) which are arranged either along a word line (WL) or along a bit line (BL) along which at least one reading operation has previously taken place are subjected to a refresh operation.

9. The method as claimed in claim 8,
wherein
the occurrence of a reading operation as such is stored as information in a flag cell (MMC) that is arranged either along a word line (WL) that is affected by the reading operation or along a bit line (BL) that is affected by the reading operation.

10. The method as claimed in claim 8 or 9,
wherein

the information stored in the affected flag cells (MMC) is reset to a standard value when carrying out the refresh operation.

11. The method as claimed in one of claims 8 to 10, wherein
the carrying-out of the refresh operation is triggered by another given event.

12. A memory arrangement having rewritable memory cells (MC) which are arranged at crossovers between word lines (WL) and bit lines (BL), in which arrangement the memory cells (MC) are configured in such a manner that the information stored in the memory cells (MC) is read out in a nondestructive manner,
wherein
- the memory arrangement has a refresh device (Refr) for carrying out a refresh operation,
- the memory arrangement has a flag cell (MMC) either for each word line (WL) or for each bit line (BL), said flag cell being able to store an item of information that indicates whether at least one of the memory cells (MC) either along the respective word line (WL) or along the respective bit line (BL) has been subjected to a reading operation since a basic state occurred, and
- the refresh device (Refr) is designed in such a manner that, for each flag cell (MMC), it carries out a refresh operation, in a manner dependent on the information stored in said flag cell (MMC), for those memory cells (MC) which are arranged along the word line (WL) or bit line (BL) associated with said flag cell (MMC).